IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Greenfield et al. Confirmation No.: 1986

Serial No: 09/186,584 Examiner: Lee, Richard J.

Filed: 11/05/98 Group Art Unit: 2613

Title: ON-CHIP DYNAMIC BUFFER LEVEL INDICATORS FOR DIGITAL VIDEO ENCODER

Declaration Under 37 C.F.R. §1.132

TO: Box AF
Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

I, Agnes Y. Ngai, declare:

1. I reside at 725 Partridge Place, Endwell, New York 13760.

2. I earned a B.S. in Electrical Engineering from the City College of New York in 1973.

3. I have worked for International Business Machines (IBM) Corporation from 1973 to the present. I have worked at IBM's Microelectronics Semiconductor Digital Video Products Group from 1992 to the present. My experience at IBM also includes working in S370 midrange processing technology, RISC processing technology, and memory subsystems. Since 1992 my work has focused on video compression and decompression development.

4. I have authored and co-authored over 40 patents and a number of publications. I am a recipient of the IBM 16th Plateau Invention Achievement Award.

5. As a co-inventor, I have reviewed and do understand the contents of the above – identified application, which is directed, in part, to a novel hardware implementation of certain features of a digital video encoding system. Further, I am a co-inventor of the applied patent issued to Greenfield et al. (U.S. Patent No. 5,760,836) and do understand the contents of that

patent. In addition, I have reviewed the Choe et al. patent (U.S. Patent No. 6,094,696), and am aware of the final Office Action mailed September 18, 2002 in connection with the above-designated application.

In support of the novelty and non-obviousness of the pending claims, I present herewith an explanation of certain features of the Greenfield et al. encoding system, and why the pending claims would not have been anticipated or obvious to myself or other experts in the field based on the applied patents.

For a teaching of my claimed concept, the Office Action relies significantly on the language at column 5, line 24-30 of Greenfield et al. ('836), where it is stated that a real-time encoding system is provided, which is repeated herein for convenience.

> Another factor which can be used to adjust the step size is the fullness of the external buffer, which in real time encoding systems is typically an external FIFO device. By monitoring the amount of data read from the FIFOs and data used to encode the bitstream (E), the bitrate can be adjusted to prevent overflow of the external buffers 51 in a normal operating environment.

The "real-time encoding system" of Greenfield et al. means that the encoder discussed therein is capable of encoding a number of pictures per second as specified by the relevant standard, which in the case of NTSC means 30 frames per second. Depending on the operating frequency of the encoder, there are thousands and thousands of cycles per picture. A real time encoding thus means that the encoder can complete the calculations or executions needed to produce, e.g., thirty frames in one second. I submit as an expert skilled in the art, that this does not mean one would read Greenfield et al. as necessarily inferring that the encoder is executing or performing the same calculation or instruction every cycle.

The method of calculating external buffer fullness disclosed by Greenfield et al. is cited at column 5, lines 50-57 to include reading the counter and FIFO configuration register using microcode. Microcode then performs the R (number of bits read by the host) calculation. The microcode also monitors the number of bits encoded, and subtracts the amount of data read by the host. The result of this calculation is the fullness of the external buffer. This teaching of

Greenfield et al. clearly states that microcode is used to monitor the external buffer fullness. Microcode performs a function, calculation of buffer fullness in this case, by executing a sequence of different instructions. One instruction may be, for instance, executed once per machine cycle. The end of the sequence of instructions produces the desired calculation. Since different instructions are executed each cycle in the sequence needed to calculate or determine buffer fullness, the microcode cannot perform a buffer fullness calculation every cycle. Because the microcode cannot provide a buffer fullness calculation every cycle, the actual fullness of the buffer is not known continuously every cycle.

The Greenfield et al. encoder does not provide any means to continuously obtain the fullness of the external buffer and does not provide a dynamic buffer level indicator in real-time (every cycle) indicative of the fullness of the external buffer. Further, there is no disclosure in Greenfield et al. that would lead me, as one skilled in the art, to expect that the hardware logic discussed therein would be capable of supporting a continuously obtaining of buffer fullness.

To summarize, the Greenfield et al. real-time encoding system employs use of microcode to update a buffer level indicator. Because microcode is employed, the buffer level signal cannot be returned on a continuous basis (i.e., in real-time), nor every machine cycle. In practice, the buffer level indicator in Greenfield et al. would, for example, be returned approximately once per macroblock. This timing issue resulted in a problem which is identified and addressed by the present application. The Greenfield et al. real-time encoding system inherently has a latency issue which produces an inaccuracy in the FIFO fullness reading because the calculations rely on microcode. Finally, I submit that the final Office Action mischaracterizes the teachings of Greenfield et al. to the extent that it relies upon the "real-time encoding system" characterization to argue that every function within the system inherently continuously occurs on every cycle. Clearly, this is impossible given the nature of software. The real-time encoding (i.e., 30 frames per second) does not equate to a continuous, dynamic indication of buffer fullness, nor more particularly, such a determination thereof every machine cycle.

I declare that all statements for the foregoing Declaration made of my own knowledge are true and that all statements made upon information and belief are believed true and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both under section 1001 of Title 18 of the United

States Code and that such willful false statements may jeopardize the validity of the above-identified application or any patent issuing thereon.

Signed by me this 18th day of November, 2002.

Agnes Y. Ngai

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